Frequency Synthesizer

DSG-3xM

Operating Manual

Rev. 1.0

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1.0	June 06, 2014	DSG-3xM Frequency Synthesizer Manual (starting from DSG-03M-RF)

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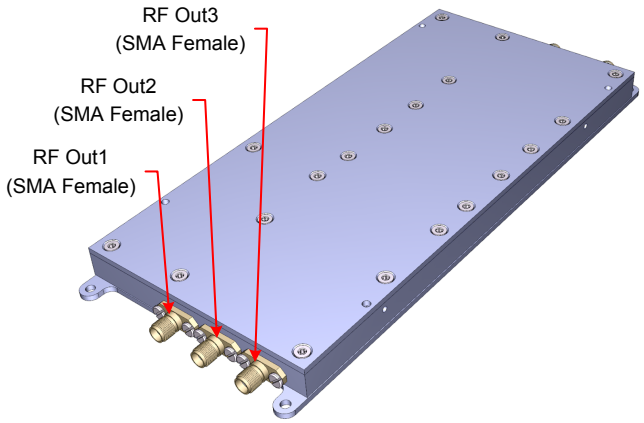

Figure 1: RF Out Connectors

1 Getting Started

1.1 Interfaces and Connectors

Synthesizer can be supplied with heatsink for better power dissipation (see HS-LNO option).

Figures 1, 2, 3 show external interfaces and connectors of DSG-3xM-RF synthesizer. The module has the following connectors:

RF Out1, RF Out2, RF Out3 – RF signal outputs, 0.5 MHz to 250 MHz frequency range with about $3.5 \cdot 10^{-6}$ Hz step, 0 to +10 dBm level range (RF Out1 and RF Out2), +3 to +13 dBm level range (RF Out3) with about 0.02 dB step, connector type – SMA, female;

REF In – input of optional external reference frequency signal, rated level 0 dBm. Signal of any frequency multiple to 1 MHz can be applied in 1 to 250 MHz range;

REF Out – output of reference frequency signal that is in use at the moment, output level about +10 dBm. If external signal is used as the reference (applied to REF In) then REF Out duplicates this signal, if internal TCXO is used, it duplicates internal reference signal (10 MHz);

SPI Control and Power Supply – SPI interface designed to control DSG module, LVTTL 3.3V levels, max. clock rate is 20 MHz (except FLASH and Temperature Sensor operations – 10 MHz). Connector type: 2 row, 2 mm pitch, 16-pin holder.

Table 1 shows pinout of SPI Control and Power Supply interface.

1.2 DSG-KIT

DSG-KIT includes DSG Frequency Synthesizer and RS2SPI evaluation board (fig. 4). It is designed for quick start and helps to understand SPI protocol com-

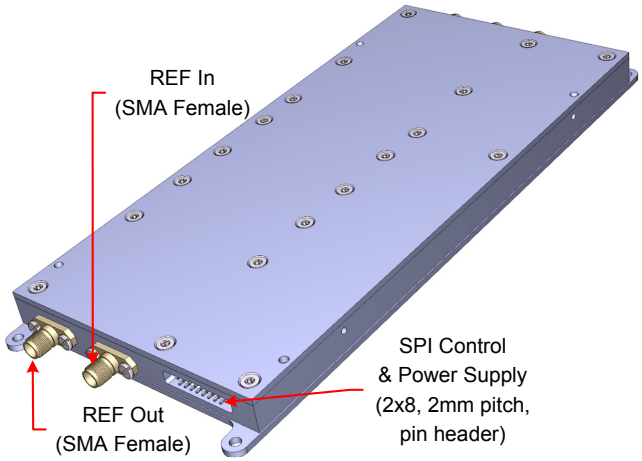

Figure 2: REF In, REF Out and SPI Connectors

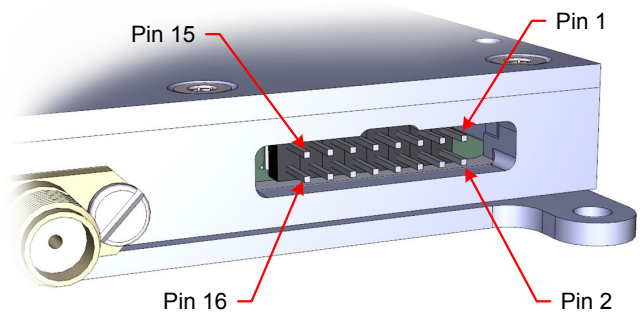

Figure 3: SPI Control and Power Supply interface

Table 1: SPI Control and Power Supply pinout

Pin #	Name	Direction (relative to module)	Description (CTL_SPI bus signals)
1	MOSI	In	SPI master output, slave input
3	SS#	In	SPI select signal, data are latched only if this signal is active (“0” state)
5	SCK	In	SPI clock signal, data are latched by rising edge of SCK signal
7	MISO	Out	SPI master input, slave output
8	AUX	Out	Buffered PLL (ADF4002) MUXOUT signal. Can be used as Interrupt signal: “0” – normal condition, “1” – PLL NOT LOCKED condition. For more details see Table 3 on page 18. AUX pin is connected to CPLD via 1 kOhm resistor, so if not used you can tie it to GND
2, 10, 12, 14, 16	GND	–	Ground pins, internally connected to the case body
4, 6	–	In	Not used, can be left unconnected or tied to ground
9, 11	+5V	In	Positive power supply, +5.0 to +5.5V allowed. Rated current 190mA
13, 15	+9V	In	Positive power supply, +9 to +12V allowed, but to reduce overheating and power consumption it’s better not to exceed +10V. Rated current 480mA

mand set and algorithms used to control DSG synthesizer. All SPI commands which sent to the module are displayed in log window of the application. So you can easily check yourself while debugging of your own control system of the synthesizer. For remote control of DSG module follow the steps below.

1. Connect DSG module to the RS2SPI board (*Connector 1* located on the top side of the board, see fig. 4) via SPI cable (16-pin, 2-mm pitch, IDC flat cable).
2. Connect RS2SPI board to PC via USB or RS-232 cable (see jumper positions for USB/RS-232 use on fig. 4)
3. Connect RS2SPI board to **+12 VDC** power supply. Max current of the power supply source should be set to **3A** for the DC-DC converters of RS2SPI board to start. Turn on the power. Power supply consumption will be about 60mA (for non-initialized DSG block).
4. When using USB cable find out the COM-port number in Computer Management window (see fig. 5) You can specify another COM-port number (Properties ▷ Port Settings ▷ Advanced ▷ COM Port Number).
5. Launch *RF Debug Application* (double click on `advantex.exe` or `advantex.tcl` if you have Tcl/Tk installed).
6. Select radio-boxes as shown on the fig. 6 (specify the connector of the RS2SPI board to which DSG is connected) and click OK.
7. Select menu Setup ▷ COM_configure (fig. 7, Item 1).
8. Specify COM-port number (fig. 8) as it was determined in fig. 5. Click OK.
9. To start working with DSG-module set Power ON checkbox (fig. 9, Item 1), press Load button (Item 6), then set RF Out ON checkbox (Item 8), specify frequency and press Load button (Items 9). After pressing Load buttons (Items 6 and 9) power consumption will increase up to 0.5A if RF Out ON checkbox is checked (i.e. output stage amplifiers are on), and 0.35A if unchecked (output stage is off). You can read internal temperature of the block by pressing Read button (Item 11).

   At normal conditions (ambient +25ºC without heatsink and airflow) the internal temperature of DSG module with RF outputs turned on reaches about +43ºC.

10. If you need to use external reference, please check the box External (frequency) (fig. 9, Item 2), set the reference frequency value (Item 3), set phase detector frequency (Item 4) and press Load button (Item 6). External frequency should be in range 1 to 250 MHz and multiple to phase detector frequency since DSG uses N-integer PLL for DDS clock. PLL loop is optimized for 10 MHz PFD frequency but other values multiple to 1MHz (starting from 1 MHz) also can be applied. To check whether the PLL in locked condition press Read button (Item 7). If PLL is not locked, please try another PFD frequency (Item 4). Usually 1MHz PFD frequency leads to DSG PLL lock.

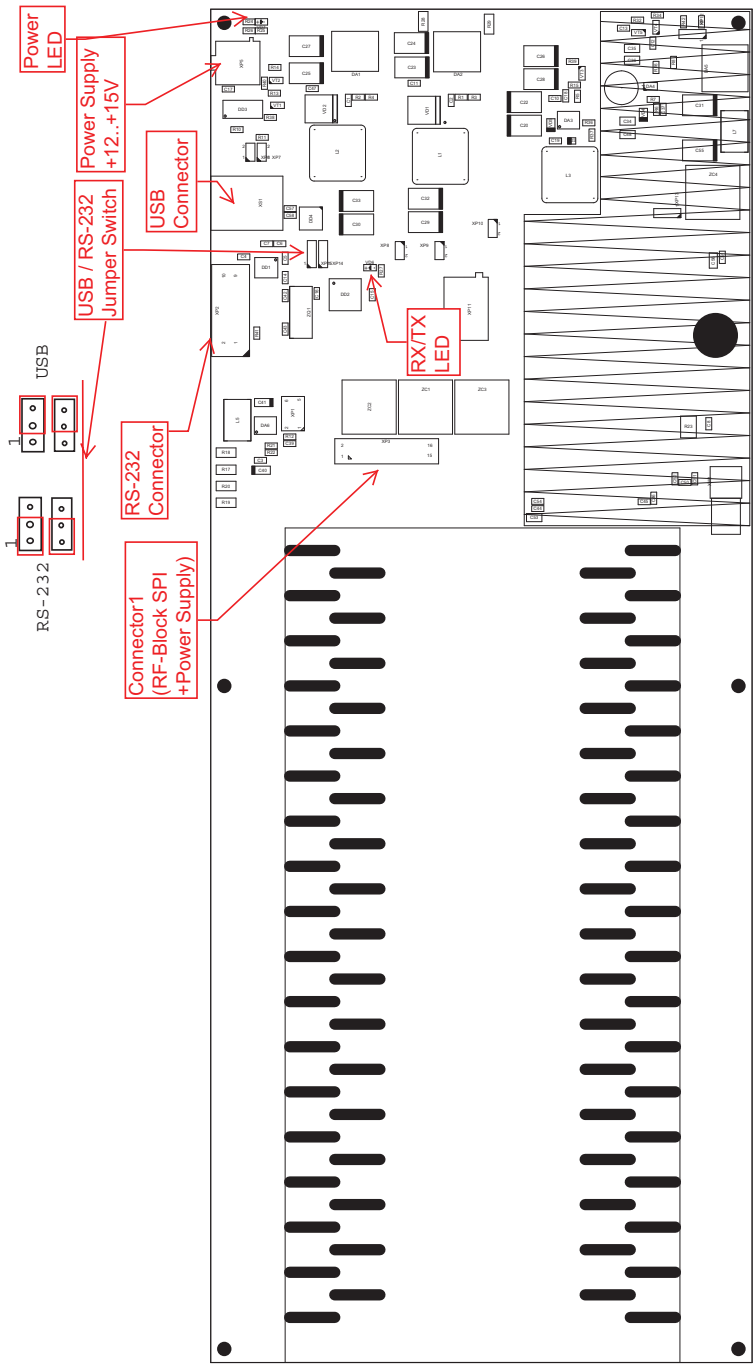

Figure 4: RS2SPI Evaluation Board

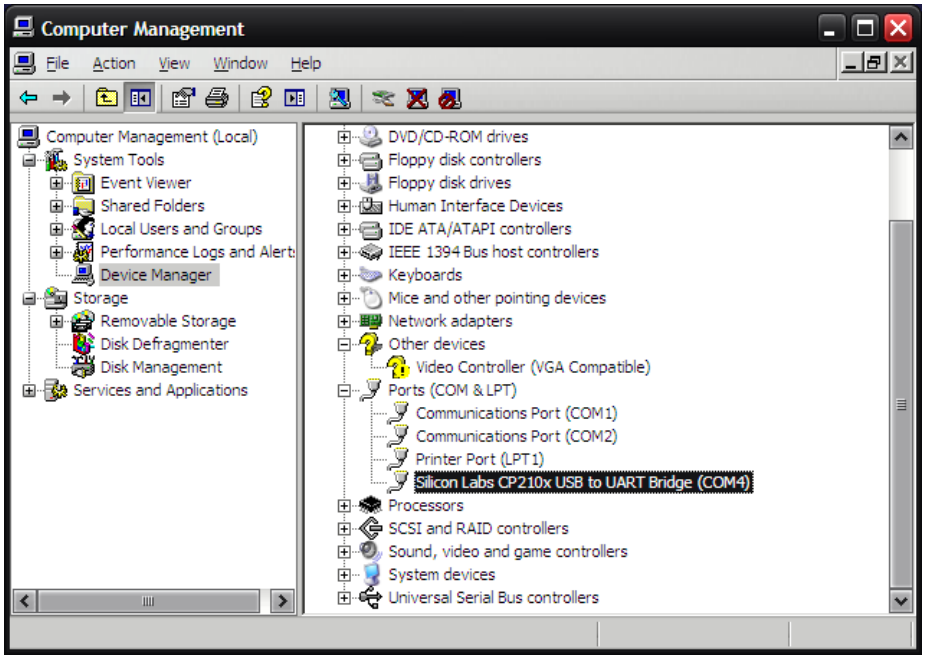

Figure 5: COM-port number

Figure 6: Select SPI-connector number

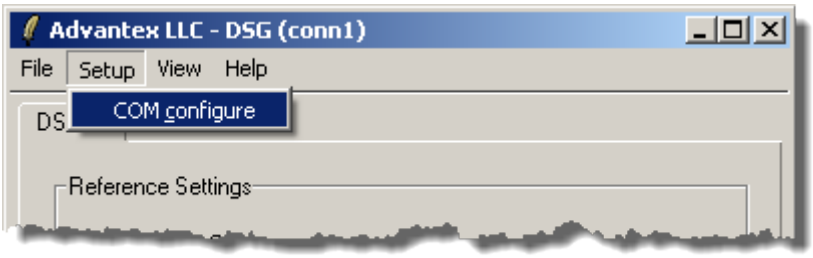

Figure 7: Main Menu

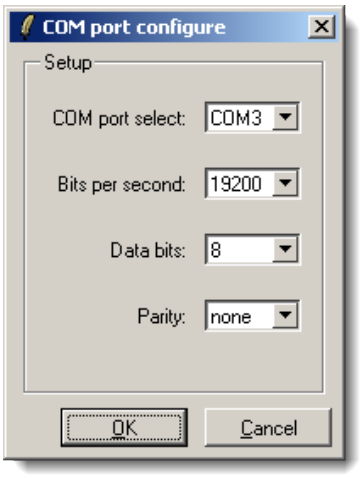

Figure 8: COM-port configuration

11. To turn on the REF Out output check ON radiobox (Item 5) and press Load button (Item 6).

12. To set output level specify DDS DAC current value and proceed with Load button (Item 10). DAC register value is in range 0 to 1023, 0 corresponds to +3 dBm and 1023 – to +13 dBm for RF Out3 output (0 to +10 for RF Out1 and RF Out2). Output signal *amplitude* is proportional to the value loaded to the DAC.

13. Log window (Item 12) shows SPI command and data values transferred to DSG while pressing Load and Read buttons.

2 SPI Command Set

2.1 General Description

DSG synthesizer does not include any MCU that would make all low-level calculations for you, just simple CPLD that works as SPI multiplexer 1-to-4 channels and contains some static registers (fig. 10). This CPLD does not use any clock signal except external SPI SCK line that changes its state only when loading new data to the DSG module. The reason of this approach is to avoid interference of MCU clock signal to analog lines and to make the response time of DSG module as fast as possible.

Figure 10 shows block diagram of DSG-3xM-RF synthesizer with internal control lines (colored in blue). There are two types of control lines: SPI channels and static registers. There is also one special line DDS_IOUPDATE which corresponds to DDS update command which toggles the corresponding DDS pin (IO_UPDATE pin of AD9912) to make new loaded in DDS data valid.

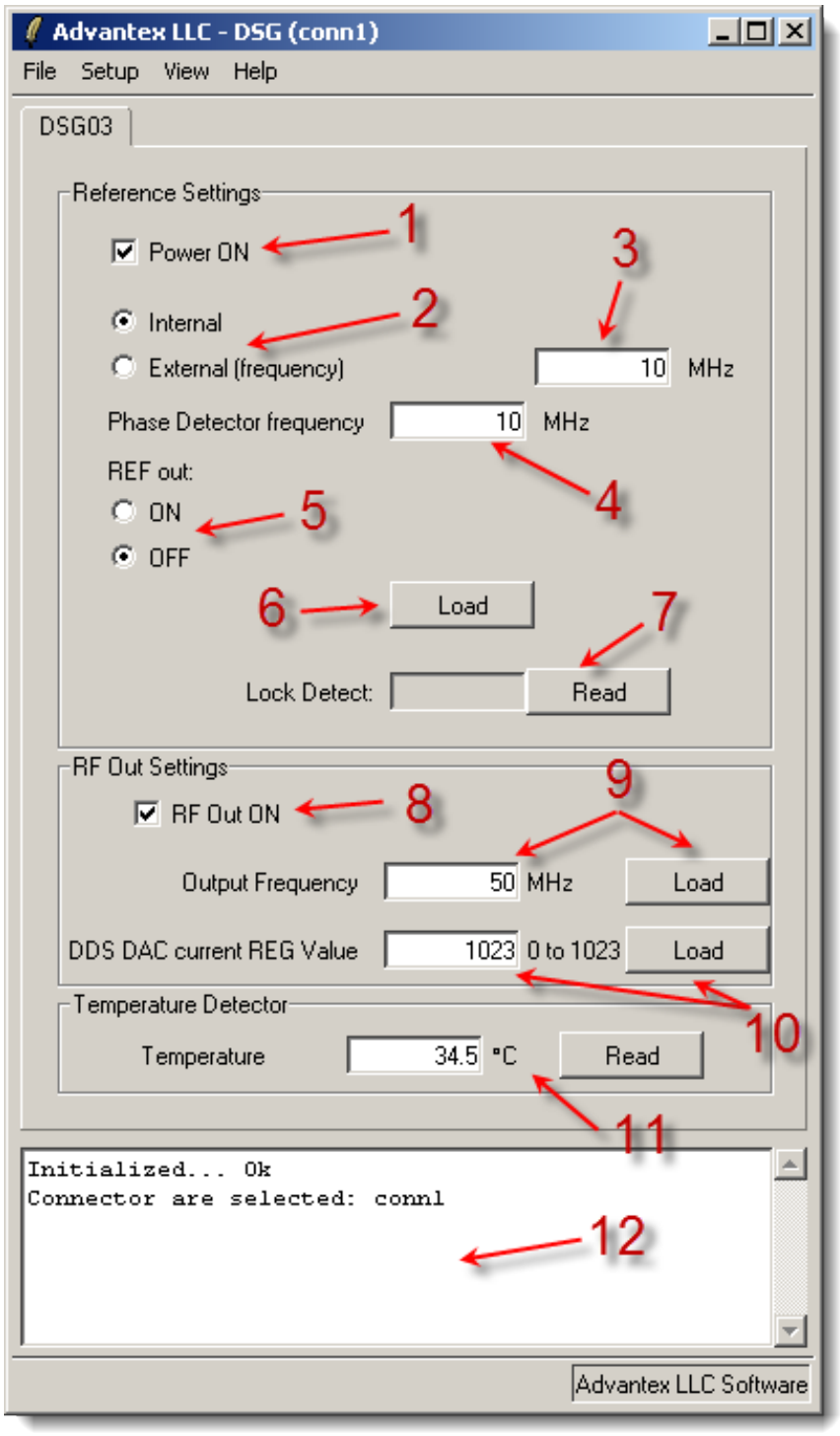

Figure 9: DSG tab

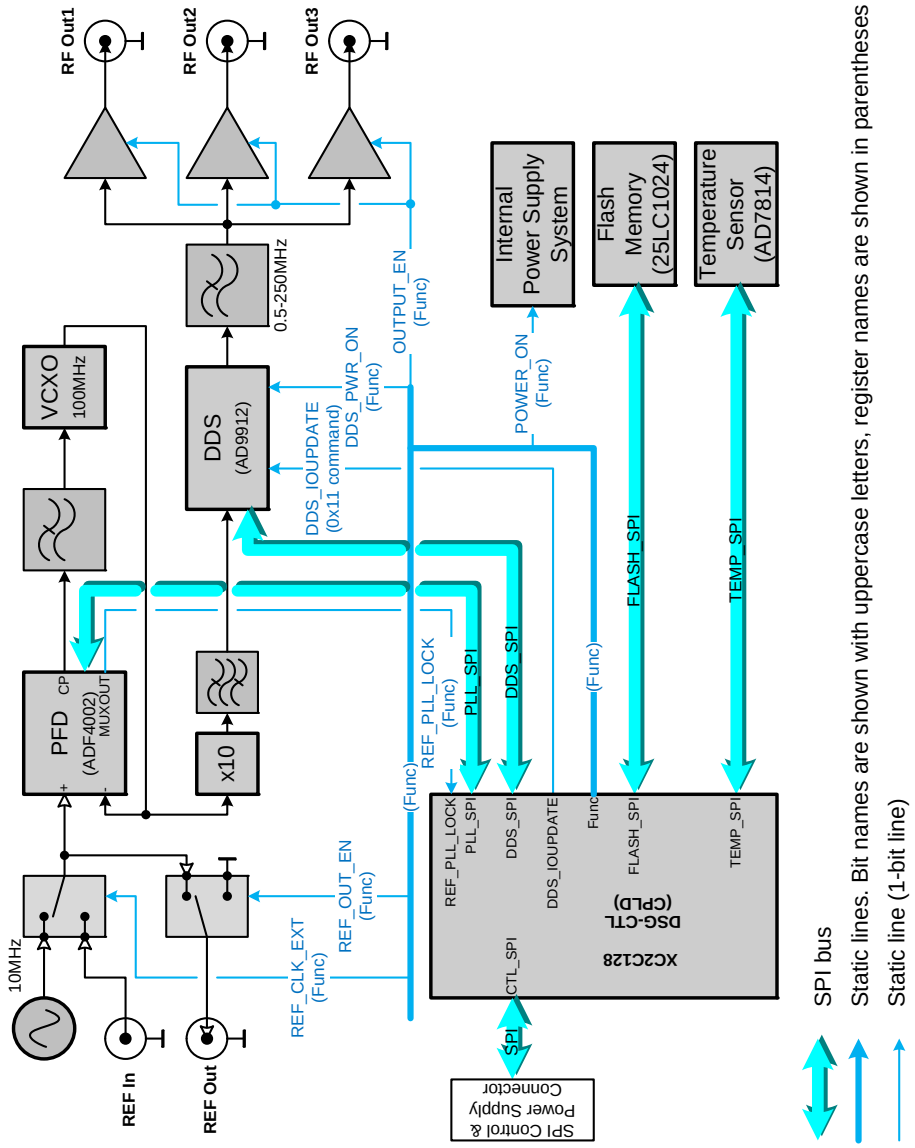

Figure 10: DSG synthesizer block diagram

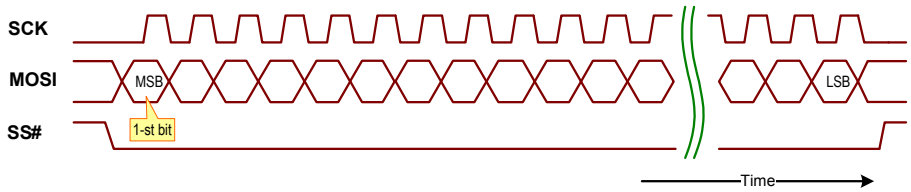

Figure 11: DSG SPI writing cycle diagram

There are four internal SPI channels:

DDS_SPI is connected to DDS (AD9912) following by filter and output amplifiers. It is used to control frequency, phase and amplitude of output signal.

PLL_SPI is connected to PLL (ADF4002) that is responsible for generating clock signal for DDS using internal or external reference.

FLASH_SPI is connected to Flash memory (25LC1024) which stores device ID data (signature, part number, serial number, date, etc.)

TEMP_SPI is connected to internal temperature sensor (AD7814) which can be used to retrieve temperature of the module.

There is one static register:

Func register is used to control internal power supply system, external reference input and output operation, AUX pin function. For more details see table 3 on page 18.

2.2 Format of SPI Commands

DSG SPI commands consist of one command byte C[7:0] following by N data bytes. Number of data bytes (N) depends on the particular command. Data on MOSI signal line are latched on rising edge of SCK signal as shown on figure 11. MSB (Most Significant Bit) is loaded first, LSB (Least Significant Bit) – last. The first is the command byte C[7:0] all other bytes are data (fig. 12). The command byte works as the address for multiplexer implemented in CPLD and defines the destination where to transfer following data – to one of the SPI channels or to one of the static registers, and the type of operation – writing or reading.

At reading cycle data on MISO line are switched on the falling edge of SCK signal and should be latched by master on rising edge of SCK signal accordingly as shown in figure 13.

2.3 SPI Commands

Table 2 shows commands C[7:0] used to control DSG module.

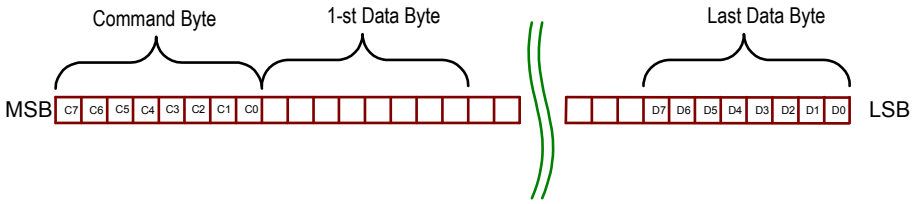

Figure 12: Command and data bytes

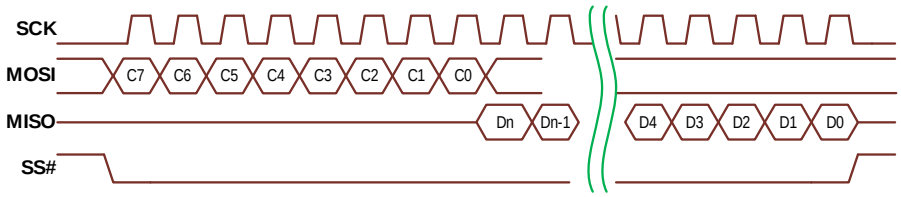

Figure 13: DSG SPI reading cycle diagram

Table 2: DSG SPI Commands C[7:0]

	C[7:0]	# of bytes	Description
1	0x01	1	Writing to Func register
2	0x81	1	Reading from Func register
3	0x10	≥ 3	Access to DDS_SPI (DDS AD9912)
4	0x11	1	Toggling DDS IO_UPDATE signal (DDS AD9912)
5	0x30	2	Access to TEMP_SPI (Temperature Sensor AD7814)
6	0x40	3	Access to PLL_SPI (PLL AD4002)
7	0x70	–	Access to FLASH_SPI (Flash Memory 25LC1024)

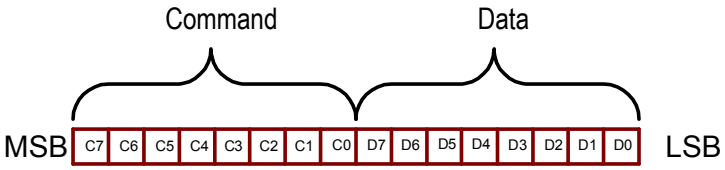

Figure 14: Writing 1 data byte

2.3.1 Func register writing C[7:0]=0x01

This command writes 1 data byte D[7:0] to Func register (fig. 14). Table 3 shows the meaning of these data bits.

2.3.2 Func register reading C[7:0]=0x81

This command reads the content of Func register. See table 3 and figure 13 for more details.

2.3.3 DDS_SPI Access C[7:0]=0x10

This command is used to access the DDS (AD9912) controlling phase, frequency and amplitude of output signal. Number of data bytes can be different but not less than 3 bytes. Actual length of data is defined in first 2 data bytes (Long Instruction). For more information refer to section 3 and AD9912 data sheet.

2.3.4 Toggling DDS_IOUPDATE C[7:0]=0x11

After DDS registers loading you need to toggle the DDS_IOUPDATE pin by sending this command to SPI.

2.3.5 TEMP_SPI Access C[7:0]=0x30

This command is used to access the temperature detector (AD7814) located near DDS IC. This command uses 2 data bytes D[15:0]. For more information refer to section 3 and AD7814 data sheet.

2.3.6 PLL_SPI Access C[7:0]=0x40

This command is used to access PLL IC (ADF4002) that is used to generate high quality clock signal for DDS. This command uses 3 data bytes D[23:0]. For more information refer to section 3 and ADF4002 data sheet.

Table 3: Func register

D7	D6	D5	D4	D3	D2	D1	D0	Description
REF_PLL_LOCK		PLL_MUXOUT_INV#	OUTPUT_EN	REF_OUT_EN	REF_CLK_EXT	DDS_PWR_ON	POWER_ON	Bit Name
0	0	0	0	0	0	0	0	Default Values
x	x	x	x	x	x	x	0	Internal Power Supply System OFF
x	x	x	x	x	x	x	1	Internal Power Supply System ON
x	x	x	x	x	x	0	x	DDS power is OFF. This also resets the DDS settings, so you need to initialyze it again after power on
x	x	x	x	x	x	1	x	DDS power is ON
x	x	x	x	x	0	x	x	Embedded TCXO (10 MHz) is used as reference frequency
x	x	x	x	x	1	x	x	External signal applied to REF In input is used as reference
x	x	x	x	0	x	x	x	REF Out output is OFF
x	x	x	x	1	x	x	x	REF Out output is ON
x	x	x	0	x	x	x	x	RF Out output is OFF
x	x	x	1	x	x	x	x	RF Out output is ON
x	x	0	x	x	x	x	x	PLL (ADF4002) MUXOUT signal is buffered to AUX with inversion
x	x	1	x	x	x	x	x	PLL (ADF4002) MUXOUT signal is buffered to AUX without inversion
0	x	x	x	x	x	x	x	PLL is not locked (Read only)*
1	x	x	x	x	x	x	x	PLL is locked (Read only)*

* For proper operation of REF_PLL_LOCK bit PLL should be programmed to fed lock detect signal to MUXOUT pin

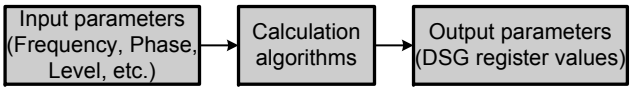

Figure 15: Input and output data for DSG programming

3 SPI Programming

3.1 Parameter Calculations

Working with synthesizer implies some calculation procedure that should be implemented on the user side. It includes algorithms of DDS FTW register value calculations based on the input frequency, etc.

Thus we have some input parameters in user friendly format (e.g. frequency, phase as float numbers), and as a result of calculation algorithms – output data in low-level format (i.e. register values), see figure 15. This section describes how to find these output parameters.

Table 4 shows input parameters. Some of them are in ready-to-use format, like power_on, output_en, ref_out_en, other can not be loaded to DSG directly. Table 5 shows intermediate variables used in calculation algorithms and output parameters which are downloaded to DSG registers.

pfd_freq

```
if(rem(ref_freq,10)==0) then //rem(X,Y) -- remainder after division X by Y
{pfd_freq=10}
elsif(rem(ref_freq,5)==0)
{pfd_freq=5}
elsif(rem(ref_freq,4)==0)
{pfd_freq=4}
elsif(rem(ref_freq,2)==0)
{pfd_freq=2}
else
{pfd_freq=1}
```

Generally the following equation can be used to find pfd_freq:

```
pfd_freq=gcd(100,ref_freq) //gcd(X,Y) -- greatest common divisor of X and Y
```

It shold be noted that loop filter phase margin is optimized for PFD frequency about 10 MHz, thus PLL *may* not be stable at pfd_freq = 20, 25, 50, 100 MHz.

r_cnt

```
r_cnt = int(ref_freq/pfd_freq)
```

Table 4: DSG input parameters

Parameter	Type	Corresponding register bits	Description
power_on	1 bit	POWER_ON (Func), DDS_PWR_ON (Func)	Turns ON/OFF DSG internal power supply system. “0” – power system is OFF (standby mode), “1” – power is ON (normal operation)
output_en	1 bit	OUTPUT_EN (Func)	Turns ON/OFF RF Out outputs. “0” – output stage is OFF, “1” – ON
ref_clk_ext	1 bit	REF_CLK_EXT (Func)	Selects reference frequency source (internal TCXO or external signal applied to REF In input). “0” – internal, “1” – external
ref_out_en	1 bit	REF_OUT_EN (Func)	Turns ON/OFF REF Out output. “0” – OFF, “1” – ON
out_freq	float	–	Frequency of output signal (at RF Out output) in MHz
v_out	float	–	Amplitude of output signal (at RF Out1 output) in V
ref_freq	float	–	Frequency of reference signal in MHz. Internal TCXO frequency is 10 MHz, external can be in range 1 to 250MHz
phase	float	–	Relative phase shift of output signal in radians. For example, if you synchronize two DSG synthesizers from the same reference source, and set the same output frequency for both of them, you can shift phase of one signal relative to another in 360 degree range

Table 5: Output parameters

Parameter / variable	Type	Description
Intermediate		
pfd_freq	float	Phase Detector frequency
Output		
r_cnt	14 bit	PLL R-counter register value (1 to 16383), [15:2] bits of Reference Counter Latch of PLL (ADF4002)
n_cnt	13 bit	PLL N-counter register value (1 to 8191), [20:8] bits of N Counter Latch of PLL (ADF4002)
ftw	48 bit	DDS Frequency Tuning Word
ptw	14 bit	DDS Phase Tuning Word
dds_fsc_reg	10 bit	Data value for DDS (AD9912) DAC full scale current, corresponds to output signal level

n_cnt

```
n_cnt = int(100/pfd_freq)
```

ftw

```
ftw = round((2^48)*out_freq/1000)
```

ptw

```
ptw = round((2^14)*phase/2π)
```

dds_fsc_reg

```
dds_fsc_reg = (1024/0.8)*(v_out-0.3)
```

where 0.3≤v_out<1.1.

3.2 Initialization

After power on the DSG synthesizer is in standby mode, i.e. internal power supply system is off, and DDS, Func and other registers are in their default state. So just after power on you need to initialize it by the following procedure.

1. Turn on the internal power supply by loading to SPI value shown in table 6. ref_out_en bit and ref_clk_sel should be set according to your needs, see table 4.

2. Turn on the DDS power supply by loading to SPI value shown in table 7. Turning on the DDS power supply as separate operation is required for all power supply voltages were settled before DDS power-on.

⚠ After DDS power on it is recommended to wait for about 50ms before loading DDS registers.

Table 6: Turning on the internal power supply system at initialization process

C[7:0]	D7	D6	D5	D4	D3	D2	D1	D0
	_	_	_	OUTPUT_EN	REF_OUT_EN	REF_CLK_EXT	DDS_POWER_ON	POWER_ON
0x01	0	0	0	0	0	0	0	1

Table 7: Turning on the DDS power supply at initialization process

C[7:0]	D7	D6	D5	D4	D3	D2	D1	D0
	_	_	_	OUTPUT_EN	REF_OUT_EN	REF_CLK_EXT	DDS_POWER_ON	POWER_ON
0x01	0	0	0	output_en	ref_out_en	ref_clk_ext	1	1

3. Initialize PLL:
   (a) 0x40007813 (Initialization Latch)
   (b) 0x40007812 (Function Latch)
   (c) 0x4012&b[r_cnt]&b00 (for internal reference pfd_freq=10MHz, r_cnt=1 thus command will be 0x40120004)
   (d) 0x40&b000&b[n_cnt]&x01 (for internal reference pfd_freq=10MHz, n_cnt=10 thus command will be 0x40000A01)


& – concatenation operator, x – hexadecimal, and b – binary designators

4. Reset the DDS – 0x10001201
5. Update DDS – 0x1100 (DDS IOUPDATE)
6. Initialize DDS:
   (a) 0x10000080 (write to DDS at address 0x0000)
   (b) 0x10001090 (write to DDS at address 0x0010)
   (c) 0x10040BFF (write to DDS at address 0x040B)
   (d) 0x10040C03 (write to DDS at address 0x040C)
7. Update DDS – 0x1100 (DDS IOUPDATE)

3.3 Setting Frequency, Phase and Level

Setting frequency:

1. 0x1061AB&b[ftw] (setting frequency)
2. 0x1100 (DDS IOUPDATE)

Setting phase offset:

1. 0x1061AD&b[ptw]
2. 0x1100 (DDS IOUPDATE)

Setting output amplitude:

1. 0x10640C[dds_fsc_reg]
2. 0x1100 (DDS IOUPDATE)

3.4 Turning ON/OFF RF Outputs

Load 0x01&b[output_en]&[ref_out_en]&[ref_clk_ext]&b11, where output_en equals 0 (outputs off) or 1 (outputs on).

Figure 16: Structure of flash-memory data transfer

3.5 Reading internal temperature

Temperature detector (AD7814) embedded to DSG calculates temperature each 350 us. Other times it resides in standby mode. If reading temperature rate is faster than 350 us then detector is not able to calculate new temperature value, and you will read the same value. Thus it is recommended to read temperature value not faster than one time per 500 us.

To read the temperature proceed as follows:

1. 0x300000 (sets normal operation of Temperature Detector)
2. Wait for 500 us
3. 0x30FFFF (sets Temperature Detector to power down mode and reads temperature code in format b00D[9:0]0000, where D is 10-bit signed integer). Temperature value in ^{o}C can be found by the following equation $T = 0.25 \cdot D$.

For more details about Temperature Detector operation see AD7814 datasheet.

3.6 Flash Memory

DSG synthesizer has 1 Mbit (131072 bytes) Flash-memory. Its address space is within 0x00000 to 0x1FFFF range. Memory space is divided into pages, 256 bytes each. It is possible to work with separate bytes and with pages. Pages start at addresses 0xXXX00, where XXX is in range 000 to 1FF. The number of data bytes in packet can be different and depends on the actual memory command. General structure of the packet is shown in figure 16. First command byte, FLASH_ADR (0x70 – Flash-memory access, see table 2), is for CPLD multiplexer, second byte is command for the 25LC1024 memory, followed by data bytes if required. Flash-memory commands are listed in table 8.

3.6.1 FLASH_CMD_READ (0x03)

Data read command, see figure 17. First byte – FLASH_SPI access command for CPLD multiplexer (0x70), second – flash data read command FLASH_CMD_READ (0x03), then three bytes which contains data address ADR[2:0]. Actually it's start address, so if you hold SS# signal in active position ("0") you will get data at next address for each CLK cycle. For example if we have the following data (3 bytes) 0xAA, 0xBB, 0xCC which are located at addresses 0x000006,

Table 8: Flash-memory commands

Command	Byte	Description
FLASH_CMD_READ	0x03	Read data
FLASH_CMD_WRITE	0x02	Write data
FLASH_CMD_WREN	0x06	Write data enable
FLASH_CMD_WRDI	0x04	Write data disable
FLASH_CMD_RDSR	0x05	Read status register
FLASH_CMD_WRSR	0x01	Write status register
FLASH_CMD_PE	0x42	Page erase
FLASH_CMD_SE	0xD8	Byte erase
FLASH_CMD_CE	0xC7	Erase all
FLASH_CMD_RDID	0xAB	Read ID and Turn on flash-memory Power Supply
FLASH_CMD_PDP	0xB9	Turn off flash-memory Power Supply

Figure 17: Flash-memory data read command

0x000007 and 0x000008 respectively. To retrieve these three bytes at once we need to send the following command: 0x0703000006000000. Last three zero bytes in this command are used to generate CLK cycles to retrieve three consecutive data bytes. As a response on MISO line we will obtain the following: 0xAABBCC.

3.6.2 FLASH_CMD_WRITE (0x02)

Data write command, see figure 18. First byte – FLASH_SPI access command for CPLD multiplexer (0x70), second – flash data write command FLASH_CMD_WRITE (0x02), then three address bytes ADR[2:0] and data bytes. First data byte will be written at ADR[2:0] address, second at ADR[2:0]+1 and so on, but all written data should reside inside the same page. This way maximum number of data bytes is 256 if ADR[2:0] points to the start of page. Otherwise if address ADR[2:0] plus number of bytes exceeds the address of end of page, some data of this page will be overwritten. This will result in lost of some data.

Figure 18: Flash-memory data write command

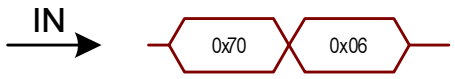

Figure 19: Flash-memory write enable command

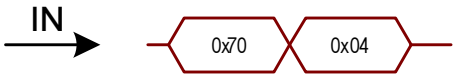

Figure 20: Flash-memory write/erase disable command

3.6.3 FLASH_CMD_WREN (0x06)

Write enable command, see figure 19. This command sets WEL bit to "1" in flash-memory status register. To enable any write or erase operation, this bit should be set to "1", otherwise these operations won't be performed. WEL bit is reset automatically to "0" after performing the following commands:

- FLASH_CMD_WRDI
- FLASH_CMD_WRSR
- FLASH_CMD_WRITE
- FLASH_CMD_PE
- FLASH_CMD_SE
- FLASH_CMD_CE

After power on WEL bit is also in "0" state.

3.6.4 FLASH_CMD_WRDI (0x04)

This command disables write and erase operations by setting WEL bit to "0" in status register of flash-memory. Command is shown in figure 20.

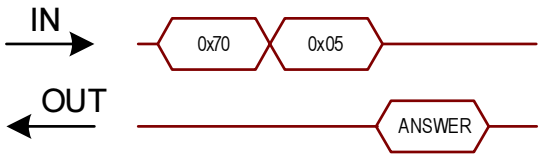

Figure 21: Flash-memory status register reading

Table 9: Flash-memory status register

	R7	R6	R5	R4	R3	R2	R1	R0
Read/Write	–	–	–	–	R/W	R/W	R	R
	X	X	X	X	BP1	BP0	WEL	WIP

Table 10: Flash-memory block protection

BP1	BP0	Protected area	Unprotected area
0	0	–	All address area (00000h-1FFFFh)
0	1	Upper 1/4 address space (18000h–1FFFFh)	Lower 3/4 address space (00000h-17FFFh)
1	0	Upper 1/2 address space (10000h-1FFFFh)	Lower 1/2 address space (00000h-0FFFFh)
1	1	All address space (00000h-1FFFFh)	–

3.6.5 FLASH_CMD_RDSR (0x05)

This command reads flash-memory status register, see figure 21. Table 9 shows the content of status register.

WIP – flash-memory busy. "1" – write operation in progress (is not finished). "0" – all operations are finished.

WEL – write enable. "0" – write/erase operation disabled, "1" – enabled.

BP1, BP0 – memory block write protection. All address space is divided into 4 blocks and these bits can be used to control protection for write/erase operations for these blocks, see table 10.

To perform reading operation you need to send 0x700500.

3.6.6 FLASH_CMD_WRSR (0x01)

Write to status register, figure 22. Actually this command is used to set BP0 and BP1 bits, since WEL bit can be controlled via FLASH_CMD_WREN and FLASH_CMD_WRDI commands.

Figure 22: Flash-memory write to status register

Figure 23: Flash-memory page erase command

Figure 24: Flash-memory byte erase command

3.6.7 FLASH_CMD_PE (0x42)

Command erases content of a page which address is inserted in command, see figure 23.

3.6.8 FLASH_CMD_SE (0xD8)

Clears one byte, figure 24.

3.6.9 FLASH_CMD_CE (0xC7)

Clears all memory, figure 25.

3.6.10 FLASH_CMD_RDID (0xAB)

This command turns on the memory power supply and reads ID number of the chip (ID=0x29), figure 26. To perform reading you should send 0x70AB00, and you get 0x29 in response.

3.6.11 FLASH_CMD_PDP (0xB9)

Turns off the memory chip power supply, see figure 27.

3.7 Memory address and data mapping

Address and data mapping is shown in table 11.

Table 11: Memory address and data mapping

Address	Variable/Value	Description

(continued on next page)

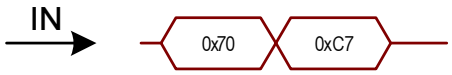

Figure 25: Flash-memory clear all command

(continued Table 11, beginning on page 28)

Address	Variable/Value	Description
0x00	0xAA	CONFIGBLKSIG0
0x01	0xBB	CONFIGBLKSIG1
0x02	0xCC	CONFIGBLKSIG2
0x03	0xDD	CONFIGBLKSIG3
0x04	PID0	Product ID (LSB)
0x05	PID1	Product ID (MSB)
0x06	SID0	Software ID (LSB)
0x07	SID1	Software ID (MSB)
0x08	SN0	Serial Number (LSB)
0x09	SN1	Serial Number (MSB)
0x0A	LOT	Lot
0x0B	DY	Year of production
0x0C	DM	Month of of production
0x0D	DD	Day of production
0x10	REF_FR0	Reference frequency in Hz (LSB)
0x11	REF_FR1	Reference frequency in Hz
0x12	REF_FR2	Reference frequency in Hz
0x13	REF_FR3	Reference frequency in Hz (MSB)
0x14	DATA_SIZE0	Size of Data Block (LSB)
0x15	DATA_SIZE1	Size of Data Block
0x16	DATA_SIZE2	Size of Data Block
0x17	DATA_SIZE3	Size of Data Block (MSB)
0x18	FLASH_SIZE0	Flash-memory size (LSB) = 0x00
0x19	FLASH_SIZE1	Flash-memory size = 0x00
0x1A	FLASH_SIZE2	Flash-memory size = 0x00
0x1B	FLASH_SIZE3	Flash-memory size (MSB) = 0x02
0x00FE	CRC0	CRC 16-bit (LSB)
0x00FF	CRC1	CRC 16-bit (MSB)
0x0100 (0xXXX00)	0x99	TABLESIG0
0x0101	0x88	TABLESIG1
0x0102	0x77	TABLESIG2
0x0103	0x66	TABLESIG3
0x0104	CTYPE	Table type (characteristic type)
0x0105	XVALUE	Type of X axis values
0x0106	YVALUE	Type of Y axis values
0x0107	ZVALUE	Type of Z axis values
0x0108	ZCOUNT0	Number of points on Z axis (LSB)

(continued on next page)

(continued Table 11, beginning on page 28)

Address	Variable/Value	Description
0x0109	ZCOUNT1	Number of points on Z axis
0x010A	ZCOUNT2	Number of points on Z axis
0x010B	ZCOUNT3	Number of points on Z axis (MSB)
0x010C	XYCOUNT0	Number of points on X axis (LSB)
0x010D	XYCOUNT1	Number of points on X axis
0x010E	XYCOUNT2	Number of points on X axis
0x010F	XYCOUNT3	Number of points on X axis (MSB)
0x0110	0x33	XROWSIG0
0x0111	0x22	XROWSIG1
0x0112	X_MULT	X multiplier
0x0113	–	Not used
0x0114	X_L0	X grid value 0 (LSB)
0x0115	X_H0	X grid value 0 (MSB)
0x0116	X_L1	X grid value 1 (LSB)
0x0117	X_H1	X grid value 1 (MSB)
0x0118	X_L2	X grid value 2 (LSB)
0x0119	X_H2	X grid value 2 (MSB)
0x011A	X_L3	X grid value 3 (LSB)
0x011B	X_H3	X grid value 3 (MSB)
0x011C	X_L4	X grid value 4 (LSB)
0x011D	X_H4	X grid value 4 (MSB)
	0x55	ZROWSIG0
	0x44	ZROWSIG1
	Z_L0	Z grid value 0 (LSB)
	Z_H0	Z grid value 0 (MSB)
	Y_L0	Y value for X grid value 0 and Z grid value 0 (LSB)
	Y_H0	Y value for X grid value 0 and Z grid value 0 (MSB)
	Y_L1	Y value for X grid value 1 and Z grid value 0 (LSB)
	Y_H1	Y value for X grid value 1 and Z grid value 0 (MSB)
	Y_L2	Y value for X grid value 2 and Z grid value 0 (LSB)
	Y_H2	Y value for X grid value 2 and Z grid value 0 (MSB)
	0x55	ZROWSIG0
	0x44	ZROWSIG1

(continued on next page)

(continued Table 11, beginning on page 28)

Address	Variable/Value	Description
	Z_L1	Z grid value 1 (LSB)
	Z_H1	Z grid value 1 (MSB)
	Y_L0	Y value for X grid value 0 and Z grid value 1 (LSB)
	Y_H0	Y value for X grid value 0 and Z grid value 1 (MSB)
	Y_L1	Y value for X grid value 1 and Z grid value 1 (LSB)
	Y_H1	Y value for X grid value 1 and Z grid value 1 (MSB)
	Y_L2	Y value for X grid value 2 and Z grid value 1 (LSB)
	Y_H2	Y value for X grid value 2 and Z grid value 1 (MSB)
0xXXXFE	CRC0	CRC 16-bit (LSB)
0xXXXFF	CRC1	CRC 16-bit (MSB)

.

Memory space is divided into two blocks: configuration block (00000h-000FFh) and data block. Data of each block is supplied with check sum (CRC). CRC for configuration block is placed at 000FEh-000FFh, CRC for data block is placed at the end of last page of data block. The address of the CRC word for data block can be found as DATASIZE[3:0]+0x100. CRC calculation algorithm is standard CCITT, 16-bit, polynomial A001h, starting with FFFFh. CRC is calculated for all data (even for unused space) that is multiple to memory page, i.e. for configuration block – from 0h to FD, and for data block – from 100h to DATASIZE[3:0]+0xFF inclusively.

3.7.1 Configuration Block

Configuration block occupies 256 bytes, from 00000h to 000FFh. First four bytes are signature of the configuration block 0xDDCCBBAA.

PID[1:0] – product ID (unsigned integer 0 to 65535), first (5-digit in DEC) number in full serial number of particular device. This ID corresponds to the part number of the device. For example for the following partnumber DSG-03M-RF the ID will be 08793, while full serial number can be 08793-4050-014.

SID[1:0] – software ID, it can be treated as version of set of calibration data tables in data block.

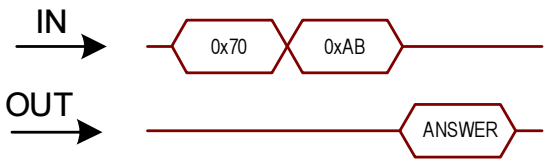

Figure 26: Flash-memory power on and read ID command

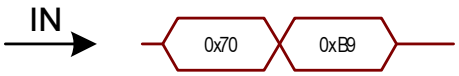

Figure 27: Flash-memory power off command

SN[1:0] – serial number (unsigned integer 0 to 999), last number (3-digit in DEC) in full serial number of particular device. It's 014 for the example above.

LOT – lot number (unsigned integer 0 to 9). Lot is coded as last digit in second digit group of full serial number, i.e. 0 in the example above.

DY – year of production starting from 1970 (unsigned integer). Thus real year is DY+1970. Last digit of the year is coded as first digit in second digit group of full serial number, i.e. 4 in the example above.

DD – day of production (unsigned integer 1 to 31).

DM – month of production (unsigned integer 1 to 12). Month is coded as 2-nd and 3-rd digits in second digit group of full serial number, i.e. 05 in the example above.

FR_REF[3:0] – reference frequency value expressed in Hz (unsigned integer, normally 147 000 000). Please note, that before using it in calculations you need to express it in MHz, i.e. you should to change its type to float and then divide this value by 1 000 000.

DATA_SIZE[3:0] – size of data block excluding its CRC (2 bytes).

FLASH_SIZE[3:0] – size of embedded flash-memory in bytes.

Unused bytes in configuration block are filled with zeroes.

3.7.2 Data block

Data block may contain one or more calibration data tables. Each table starts with new page. The structure of the table is described below.

First 4 bytes (TABLESIG[3:0]) of the table are signature 0x66778899.

Table 12: Type of Data Table (CTYPE)

CTYPE	Description
0	Type is undefined
0x08	Calibration data for output level*
0x0A	Calibration data for DDS SpurKiller. Used to suppress some low-order spurs*

* Currently not used

Table 13: X,Y and Z-data format (XVALUE, YVALUE, ZVALUE)

{X|Y|Z}VALUE	Description
0	Type is not defined
1	2-byte integer
2	2D.2 - fixed point (2 digits after point) value, 2-byte. To convert it to float you should divide it by 100.0

Type of data table (CTYPE) The signature is followed by type of data table (CTYPE), the description is shown in table 12.

Tables with different types can be placed in memory in any order. Tables are optional.

For CTYPE=0x08 table X-data are frequency grid, normally it's not regular. X-data values are expressed in MHz. Z-data are power level grid values, normally it's regular: from 0 to +10 dBm with 2 dB step. Values are in dBm. Y-data are calibrated DAC values (2-byte unsigned integer) which correspond to the appropriate frequency (X-data value in MHz) and level (Z-data value in dBm). Y-data values should be decoded as follows:

- 0xFFFF – calibration point is not valid, it can't be used in interpolation algorithm.
- 0xFFFF > Y-data > 0x7FFF – calibration point can be used in interpolation algorithm, but its precision is not guaranteed.
- Y-data ≤ 0x7FFF – calibration point is valid and can be used in interpolation algorithm.

X,Y,Z-data type (XVALUE, YVALUE, ZVALUE) Table 13 shows types of X, Y and Z-data values.

Number of Z-data points (ZCOUNT[3:0]) 4-byte integer. It is the number of Z-axis grid points.

Number of X and Y-data points per row (XYCOUNT[3:0]) 4-byte integer. It is the number of X-axis grid points, and it is equal to number of Y-data points per row (i.e. per one Z-data value).

X-data value multiplier (X_MULT) Actually it is commonly used for frequency data. If this value equals 6 then X-data (frequency) is expressed in MHz, if 3 – in kHz, 0 – in Hz.

X_H[XYCOUNT-1:0] and X_L[XYCOUNT-1:0] MSB and LSB bytes of X-axis grid values. Usually they are frequency values.

ZROWSIG[1:0] Each data row starts with signature ZROWSIG[1:0]=0x4455.

Z_H[ZCOUNT-1:0] and Z_L[ZCOUNT-1:0] Z_H[N] and Z_L[N] are MSB and LSB bytes of Z-value for the following by Y-data Y_H[XYCOUNT-1:0,N] and Y_L[XYCOUNT-1:0,N].

Y_H[XYCOUNT-1:0] and Y_L[XYCOUNT-1:0] Z-value is followed by Y-data row.